Local Oscillator Generation Scheme in 0.18 μm CMOS for Low-IF and Direct Conversion Architectures

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Abstract — **A fully-integrated, ratio-based local oscillator (LO) generation scheme using regenerative division is described. Using 0.18 μm CMOS technology, the core LO system consumes 27 mW from a 1.8 V supply. The entire chip is fully integrated, including on-chip spiral inductors; harmonic rejection mixers are also employed to suppress unwanted mixing products to better than -36 dBc. Across a bandwidth of 150 MHz, centered at 1.63 GHz, a quadrature phase error of less than 2° and a maximum image suppression of 36 dB is achieved. Using a 4/3 multiplication factor to generate the local oscillator, LO-RF interactions are reduced and an LO-RF leakage of -86 dBm has been measured at the mixer input. This system can be utilized in low-IF or direct conversion architectures.**

I. Introduction

The demand to provide low cost wireless solutions has created much interest in direct conversion architectures. Furthermore, with the long term goal of integrating digital processing on-chip, CMOS is the technology of choice.

Designing a fully-integrated direct conversion receiver in CMOS is not without challenges. In a direct conversion receiver, the local oscillator operates at the same frequency as the received carrier. Thus RF-LO leakage can couple to the on-chip voltage controlled oscillator (VCO) and degrade receiver performance, especially in phase-modulated systems. LO-RF leakage through the substrate can cause LO re-radiation and produce undesirable DC offsets. Furthermore, CMOS technology offers passive components with low quality factor and low self-resonant frequencies, which can pose problems for the realization of higher frequency (eg. 5 GHz) designs. As such, careful LO planning is essential to the design of a direct conversion receiver.

This paper describes the design of a fractional-based LO generation scheme in a 1.8 V, 0.18 μm, single-poly, 6-metal bulk CMOS process for direct conversion or low-IF architectures. On-chip spiral inductors and harmonic-rejection mixers are used to suppress unwanted mixing products. The LO system is implemented along with direct down-conversion mixers to facilitate testing.

II. LO Generation

In [1] and [2], an offset LO scheme is described whereby a 2/3 multiplication factor is used for the GSM band and a 4/3 multiplication factor for the DCS/PCS band. For frequency and phase modulated signals, the down-conversion must be done in quadrature to retain all information. Since the LO is not generated in quadrature, a polyphase circuit is inserted in the received RF signal path; this polyphase would add loss and noise to the system [3].

An LO scheme based on regenerative division, also utilizing a 4/3 multiplication factor, is described in [4] and [5]. The architecture of a system based on regenerative division is shown in Fig. 1. This architecture requires a polyphase filter at the output to generate quadrature LO.

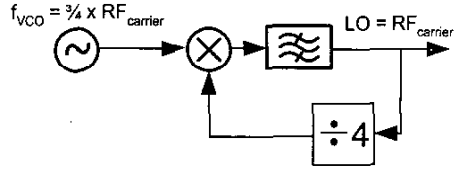

Fig. 1. Regenerative divider for VCO frequency at ¾ $RF_{carrier}$.

The proposed LO generation system, which also uses the technique of regenerative division [6], provides quadrature LO signals (a polyphase filter at the output is not needed) and employs harmonic-rejection mixers (HRM) [7]. This architecture is shown in Fig. 2. All signal paths are fully differential.

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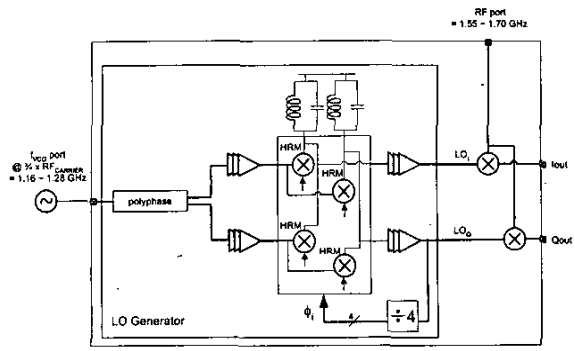

Fig. 2. System diagram of down-converter using LO generation scheme.

III. LO CIRCUITRY

A. Polyphase Filter

The VCO frequency is applied to the f_{VCO} port at 3/4 times the RF carrier frequency. A stagger-tuned four-stage polyphase filter is used to generate quadrature signals from 600 to 1795 MHz. To account for the loss of the polyphase filter, it is followed by a gain stage, which consists of a common-source, differential amplifier. This is shown in Fig. 3.

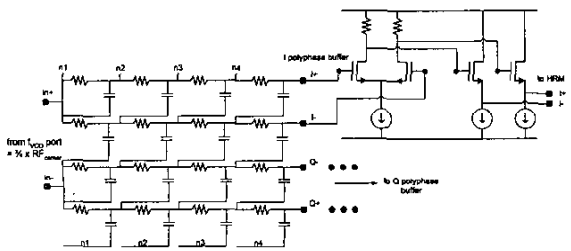

Fig. 3. Circuit diagram of 4-section polyphase filter and gain stage.

B. Harmonic Rejection Mixers

A divide-by-four circuit is used in feedback with a set of mixers to generate the 4/3 multiplication factor. A tuned LC tank forms the load for the HRMs and is used to suppress the unwanted mixing products generated as a result of the harmonics produced by the divide-by-four circuit. An 8.2 nH inductor with a quality factor of 4.5 was designed, using ASITIC [8]. HRMs were employed, to relax the filtering requirements of the LC tank. The HRM reduces the mixer products generated by the 3rd and 5th harmonics of the divide-by-four circuit. The HRMs are based on Gilbert-cell mixers as shown in Fig. 4. The phase delayed signals (Φ_i) required by the HRMs are naturally provided by the divide-by-four circuit. The Φ_i signals are weighted and delayed, as described in [7], to achieve correct harmonic cancellation.

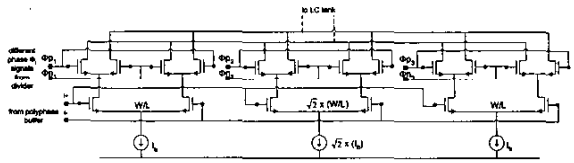

Fig. 4. Circuit diagram of harmonic-rejection mixer.

The inputs to the HRM are applied in quadrature to two sets of HRM pairs. This reduces various mixer products and also provides quadrature LO outputs. The quadrature LO signals are applied to a pair of down-conversion mixers, which provide baseband in-phase and quadrature outputs.

IV. MEASURED RESULTS

A die photo of the implemented system is shown in Fig. 5. The system, excluding the pad frame, occupies an area of approximately 1.5 mm^2.

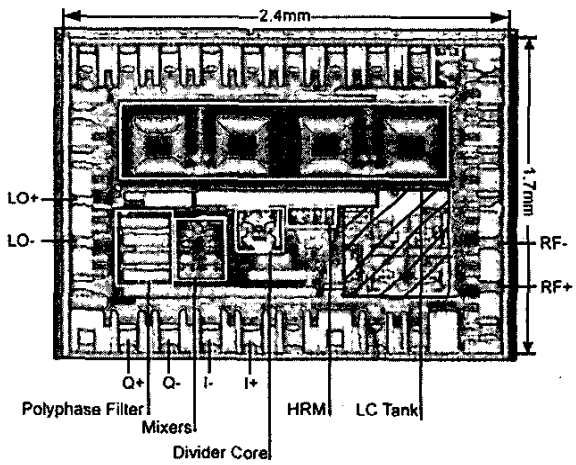

Fig. 5. Die photo of LO generation system and down-conversion mixers.

Across an input f_{VCO} range of 1.16 to 1.28 GHz (equivalent to the down-conversion of an RF band between 1.55 to 1.70 GHz), the measured quadrature error is shown in Fig. 6. All data is plotted versus the frequency that was applied to the f_{VCO} port of the chip.

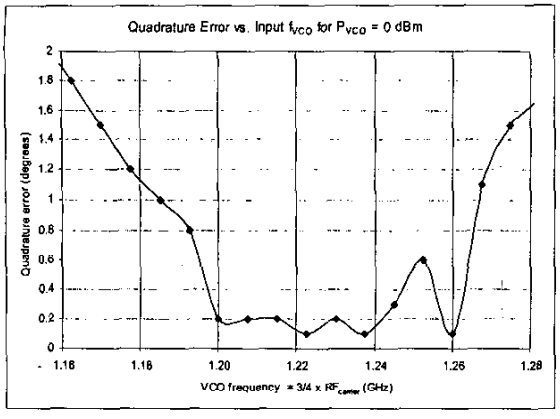

Fig. 6. Quadrature error vs. input LO frequency.

A quadrature error of less than 2° is achieved over the entire frequency range.

This system could also be used in a low-IF architecture. The equivalent unwanted image suppression of this down-conversion system has been calculated based on the measured phase and amplitude mismatch, and is shown in Fig. 7.

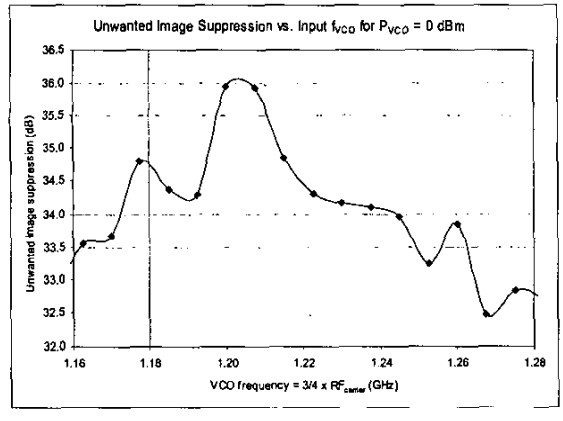

Fig. 7. Calculated unwanted image suppression vs. input LO frequency.

As stated, the HRMs are utilized to reduce the mixer products generated as a result of the 3rd and 5th harmonic outputs from the divide-by-four circuit. These are situated at 3/4 x $RF_{carrier}$ and 5/4 x $RF_{carrier}$, and mix with the input LO, at 3/4 x $RF_{carrier}$ to generate unwanted products at the following fractions of the $RF_{carrier}$: 1/2, 3/2, and 2; these products were measured to be -36 dBc, -51 dBc, and -49 dBc, respectively.

A. Results Summary

TABLE I
SUMMARY OF MEASURED RESULTS

Total power consumption at 1.8 V	45 mW
Core LO circuit power consumption at 1.8 V	27 mW
RF band	1.55 ~ 1.70 GHz
f_{VCO} range required	1.16 ~ 1.28 GHz
Quadrature error (P_{VCO} = 0 dBm)	< 2°
Amplitude mismatch (P_{VCO} = 0 dBm)	< 0.37 dB
Equivalent Unwanted Image Suppression	> 32 dB
LO-RF leakage (0 dBm applied at 1.23 GHz)	-86 dBm at 1.64 GHz at mixer inputs
RF-LO leakage (-10 dBm at 1.64 GHz)	-72 dBm
Harmonic rejection at: 1/2 x $RF_{carrier}$	-36 dBc
3/2 x $RF_{carrier}$	-51 dBc
2 x $RF_{carrier}$	-49 dBc
Circuit Area (excluding pad frame)	1.5 mm^2
Technology	0.18 µm CMOS

A VCO frequency of 3/4 x $RF_{carrier}$, or 1.16 to 1.28 GHz, is needed, to operate in an RF band from 1.55 to 1.70 GHz and generate the required LO for direct conversion or low-IF architectures. A phase error of less than 2°, with greater than an equivalent 32 dB image suppression is achieved across this band. An LO-RF leakage of -86 dBm was measured at the mixer input ports. This was achieved in a 1.8 V, 0.18 µm, single-poly, 6-metal bulk CMOS process.

V. CONCLUSION

This paper describes the implementation of a ratio-based LO generation scheme in a 1.8 V, 0.18 µm, single-poly, 6-metal bulk CMOS process for direct conversion or low-IF architectures. On-chip spiral inductors and harmonic-rejection mixers are used to improve the spurious response.

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